

This chapter describes the high-speed differential I/O features and resources, the functionality of the serializer/deserializer (SERDES), and the dynamic phase alignment (DPA) circuitry in Arria® II devices.

This chapter contains the following sections:

- “LVDS Channels” on page 8–2
- “LVDS SERDES and DPA Block Diagram” on page 8–7
- “Differential Transmitter” on page 8–8
- “Differential Receiver” on page 8–11
- “Programmable Pre-Emphasis and Programmable V_{OD} .” on page 8–10
- “Differential I/O Termination” on page 8–20
- “PLLs” on page 8–21
- “LVDS and DPA Clock Networks” on page 8–21
- “Source-Synchronous Timing Budget” on page 8–23
- “Differential Pin Placement Guidelines” on page 8–27
- “Setting Up an LVDS Transmitter or Receiver Channel” on page 8–36

Arria II devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment block (bit slip)
- DPA block
- Synchronizer (FIFO buffer)

Arria II devices support the following high-speed differential I/O standards:

- LVDS
- mini-LVDS
- RSDS
- LVPECL
- Bus LVDS (BLVDS) for Arria II GX devices



True mini-LVDS and RSDS inputs are not supported. The LVPECL I/O standard is only used for phase-locked loop (PLL) clock inputs in differential mode.

- For specifications and features of the differential I/O standards supported in Arria II devices, refer to the *I/O Features in Arria II Devices* and *Arria II Devices Data Sheet* chapters.

LVDS Channels

In Arria II GX devices, there are true LVDS input buffers and LVDS I/O buffers at the top, bottom, and right side of the device. The LVDS input buffers have 100- Ω on-chip differential termination (R_D OCT) support. You can configure the LVDS I/O buffers as either LVDS input (without R_D OCT) or true LVDS output buffers. You can also configure the LVDS pins on the top, bottom, and right sides of the device, as emulated LVDS output buffers, which use two single-ended output buffers with an external resistor network to support LVDS, mini-LVDS, and RSFS standards.

The Arria II GZ devices support LVDS on both row and column I/O banks. Row I/Os support true LVDS input with 100- Ω R_D OCT and true LVDS output buffers. Column I/Os support true LVDS input buffers without R_D OCT. You can also configure the row and column LVDS pins as emulated LVDS output buffers that use two single-ended output buffers with an external resistor network to support LVDS, mini-LVDS, and RSFS standards. Arria II GZ devices offer single-ended I/O `refclk` support for the LVDS.

Dedicated SERDES and DPA circuitries are implemented on the right I/O banks of Arria II GX devices and row I/O banks of Arria II GZ devices to further enhance the LVDS interface performance in the device. For column I/O banks in Arria II devices, SERDES is implemented in the core logic because there is no dedicated SERDES circuitry.

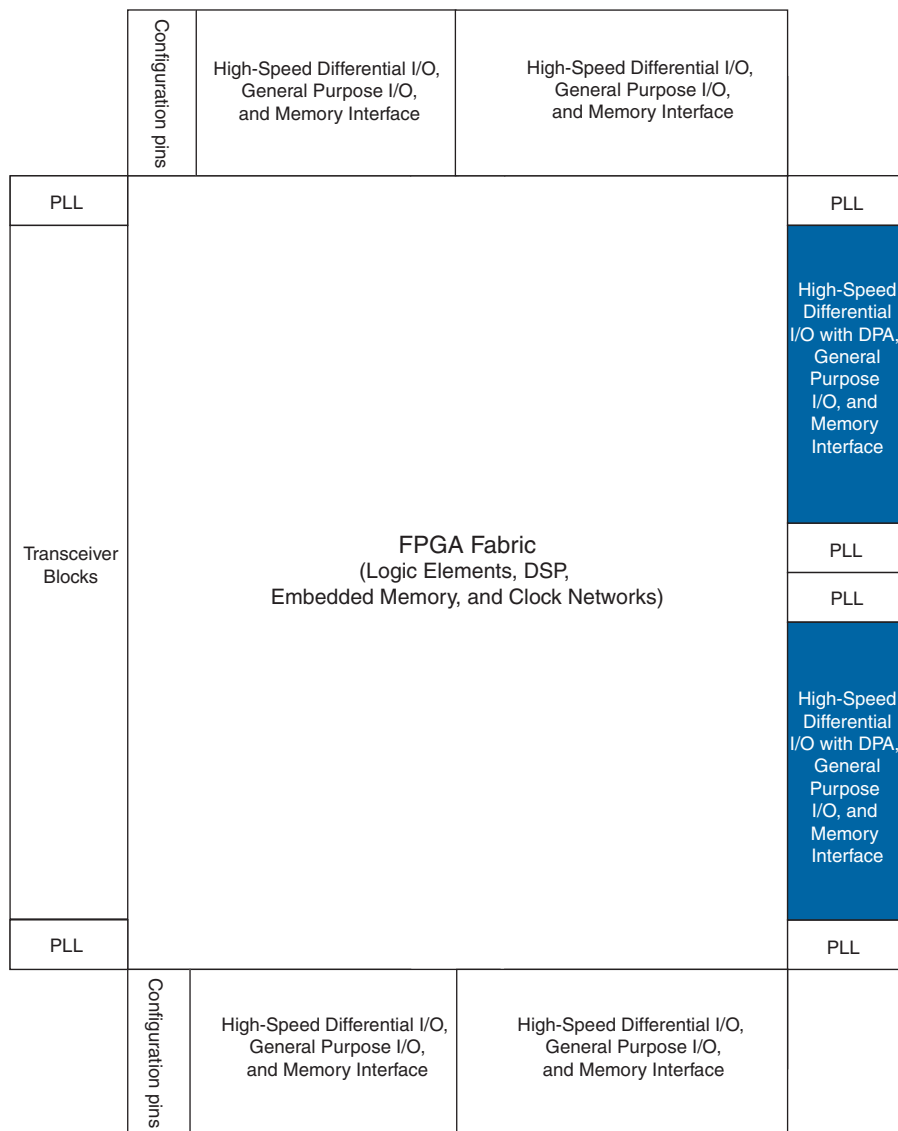
- When you configure the I/O buffers as LVDS input with R_D OCT enabled, you must set both V_{CCIO} and V_{CCPD} to 2.5 V.
- For more information about I/O banks, refer to the *I/O Features in Arria II Devices* chapter.

Locations of the I/O Banks

Arria II I/Os are divided into 16 to 20 I/O banks. For Arria II GX devices, the high-speed differential I/Os are located at the right side of the device. For Arria II GZ devices, the high-speed differential I/Os are located at the right and left sides of the device.

Figure 8-1 and Figure 8-2 show a high-level chip overview of Arria II devices.

Figure 8-1. High-Speed Differential I/Os with DPA Block Locations in an Arria II GX Device (Note 1), (2), (3)

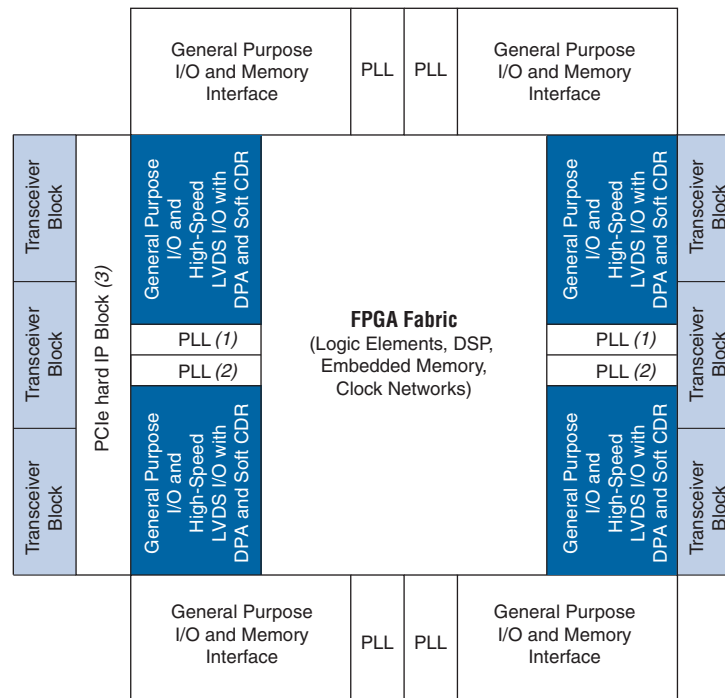


Notes to Figure 8-1:

- (1) This figure is a top view of the silicon die, which corresponds to a reverse view for flip chip packages. It is a graphical representation only.
- (2) Applicable to EP2AGX95, EP2AGX125, EP2AGX190, and EP2AGX260 devices.
- (3) There are no center PLLs on the right I/O banks for EP2AGX45 and EP2AGX65 devices.

Figure 8-2 shows a high-level chip overview of the Arria II GZ devices.

Figure 8-2. High-Speed Differential I/Os with DPA Block Locations in Arria II GZ Devices



Notes to Figure 8-2:

- (1) Not available for F780 device package.
- (2) Not available for F780 and F1152 device packages.
- (3) The PCIe hard IP block is located on the left side of the device only (IOBANK_QL).

Table 8-1 to Table 8-4 list the maximum number of row and column LVDS I/Os supported in Arria II devices. You can design the LVDS I/Os as true LVDS input, output buffers, or emulated LVDS output buffers, if the combination does not exceed the maximum count. For example, there are a total of 56 LVDS pairs of I/Os in 780-pin EP2AGX45 device row (refer to Table 8-1). You can design up to a maximum of either:

- 28 true LVDS input buffers with R_D OCT and 28 true LVDS output buffers
- 56 LVDS input buffers of which 28 are true LVDS input buffers with R_D OCT and 28 requires external 100- Ω termination
- 28 true LVDS output buffers and 28 emulated LVDS output buffers
- 56 emulated LVDS output buffers


 Dedicated SERDES and DPA circuitry are only available on the right side of the device in row I/O banks. SERDES with DPA receivers are only available on differential pins in the row I/O banks and SERDES transmitters are only available on transmit (Tx) pins in the row I/O banks. The receive (Rx) pins in row I/O banks are receiver channels without dedicated SERDES and DPA circuitry.

Table 8-1. LVDS Channels Supported in Arria II GX Device Row I/O Banks (Note 1), (2), (3), (4), (5), (6)

Device	358-Pin FlipChip UBGA	572-Pin FlipChip FBGA	780-Pin FlipChip FBGA	1152-Pin FlipChip FBGA
EP2AGX45	8(R _D or eTx) + 8(Rx, Tx or eTx)	24(R _D or eTx) + 24(Rx, Tx, or eTx)	28(R _D or eTx) + 28(Rx, Tx, or eTx)	—
EP2AGX65	8(R _D or eTx) + 8(Rx, Tx, or eTx)	24(R _D or eTx) + 24(Rx, Tx, or eTx)	28(R _D or eTx) + 28(Rx, Tx or eTx)	—
EP2AGX95	—	24(R _D or eTx) + 24(Rx, Tx or eTx)	28(R _D or eTx) + 28(Rx, Tx or eTx)	32(R _D or eTx) + 32(Rx, Tx, or eTx)
EP2AGX125	—	24(R _D or eTx) + 24(Rx, Tx or eTx)	28(R _D or eTx) + 28((Rx, Tx or eTx)	32(R _D or eTx) + 32(Rx, Tx or eTx)
EP2AGX190	—	—	28(R _D or eTx)+ 28(Rx, Tx or eTx)	48(R _D or eTx) + 48(Rx, Tx or eTx)
EP2AGX260	—	—	28(R _D or eTx) + 28(Rx, Tx or eTx)	48(R _D or eTx) + 48(Rx, Tx or eTx)

Notes to Table 8-1:

- (1) Dedicated SERDES and DPA circuitry only exist on the right side of the device in the Row I/O banks.
- (2) R_D = True LVDS input buffers with R_D OCT support and dedicated SERDES receiver channel with DPA circuitry.
- (3) Rx = True LVDS input buffers without R_D OCT support and dedicated SERDES receiver channel with DPA circuitry.
- (4) Tx = True LVDS output buffers and dedicated SERDES transmitter channel.
- (5) eTx = Emulated LVDS output buffers, either LVDS_E_3R or LVDS_E_1R.
- (6) The LVDS channel count does not include dedicated clock input pins and PLL clock output pins.

Table 8-2. LVDS Channels Supported in Arria II GX Device Column I/O Banks (Note 1), (2), (3), (4), (5), (6) (Part 1 of 2)

Device	358-Pin FlipChip UBGA	572-Pin FlipChip FBGA	780-Pin FlipChip FBGA	1152-Pin FlipChip FBGA
EP2AGX45	25(R _D or eTx) + 24(Rx, Tx, or eTx)	33(R _D or eTx) + 32(Rx, Tx, or eTx)	57(R _D or eTx) + 56(Rx, Tx, or eTx)	—
EP2AGX65	25(R _D or eTx) + 24(Rx, Tx, or eTx)	33(R _D or eTx) + 32(Rx, Tx, or eTx)	57(R _D or eTx) + 56(Rx, Tx, or eTx)	—
EP2AGX95	—	33(R _D or eTx) + 32(Rx, Tx, or eTx)	57(R _D or eTx) + 56(Rx, Tx, or eTx)	73(R _D or eTx) + 72(Rx, Tx, or eTx)
EP2AGX125	—	33(R _D or eTx) + 32(Rx, Tx, or eTx)	57(R _D or eTx) + 56(Rx, Tx, or eTx)	73(R _D or eTx) + 72(Rx, Tx, or eTx)
EP2AGX190	—	—	57(R _D or eTx) + 56(Rx, Tx, or eTx)	97(R _D or eTx) + 96(Rx, Tx, or eTx)

Table 8-2. LVDS Channels Supported in Arria II GX Device Column I/O Banks (Note 1), (2), (3), (4), (5), (6) (Part 2 of 2)

Device	358-Pin FlipChip UBGA	572-Pin FlipChip FBGA	780-Pin FlipChip FBGA	1152-Pin FlipChip FBGA
EP2AGX260	—	—	57(R _D or eTx) + 56(Rx, Tx, or eTx)	97(R _D or eTx) + 96(Rx, Tx, or eTx)

Notes to Table 8-2:

- (1) There are no dedicated SERDES and DPA circuitry in device column I/O banks.
- (2) R_D = True LVDS input buffers with R_D OCT support.
- (3) Rx = True LVDS input buffers without R_D OCT support.
- (4) Tx = True LVDS output buffers.
- (5) eTx = Emulated LVDS output buffers, either LVDS_E_3R or LVDS_E_1R.
- (6) The LVDS channel count does not include dedicated clock input pins and PLL clock output pins.

Table 8-3 and Table 8-4 list the maximum number of row and column LVDS I/Os supported in Arria II GZ devices.

Table 8-3. LVDS Channels Supported in Arria II GZ Device Row I/O Banks (Note 1), (2), (3)

Device	780-Pin FineLine BGA	1152-Pin FineLine BGA	1517-Pin FineLine BGA
EP2AGZ225	—	42(Rx or eTx) + 44(Tx or eTx)	86(Rx or eTx) + 88(Tx or eTx)
EP2AGZ300	—	42(Rx or eTx) + 44(Tx or eTx)	86(Rx or eTx) + 88(Tx or eTx)
EP2AGZ350	—	42(Rx or eTx) + 44(Tx or eTx)	86(Rx or eTx) + 88(Tx or eTx)

Notes to Table 8-3:

- (1) Rx = true LVDS input buffers with R_D OCT, Tx = true LVDS output buffers, eTx = emulated LVDS output buffers (either LVDS_E_1R or LVDS_E_3R).
- (2) The LVDS Rx and Tx channels are equally divided between the left and right sides of the device, except for the devices in the 780-pin Finline BGA. These devices have the LVDS Rx and Tx located on the left side of the device.
- (3) The LVDS channel count does not include dedicated clock input pins.

Table 8-4. LVDS Channels Supported in Arria II GZ Device Column I/O Banks (Note 1), (2), (3)

Device	780-Pin FineLine BGA	1152-Pin FineLine BGA	1517-Pin FineLine BGA
EP2AGZ225	—	93(Rx or eTx) + 96 eTx	93(Rx or eTx) + 96 eTx
EP2AGZ300	68(Rx or eTx) + 72 eTx	93(Rx or eTx) + 96 eTx	93(Rx or eTx) + 96 eTx
EP2AGZ350	68(Rx or eTx) + 72 eTx	93(Rx or eTx) + 96 eTx	93(Rx or eTx) + 96 eTx

Notes to Table 8-4:

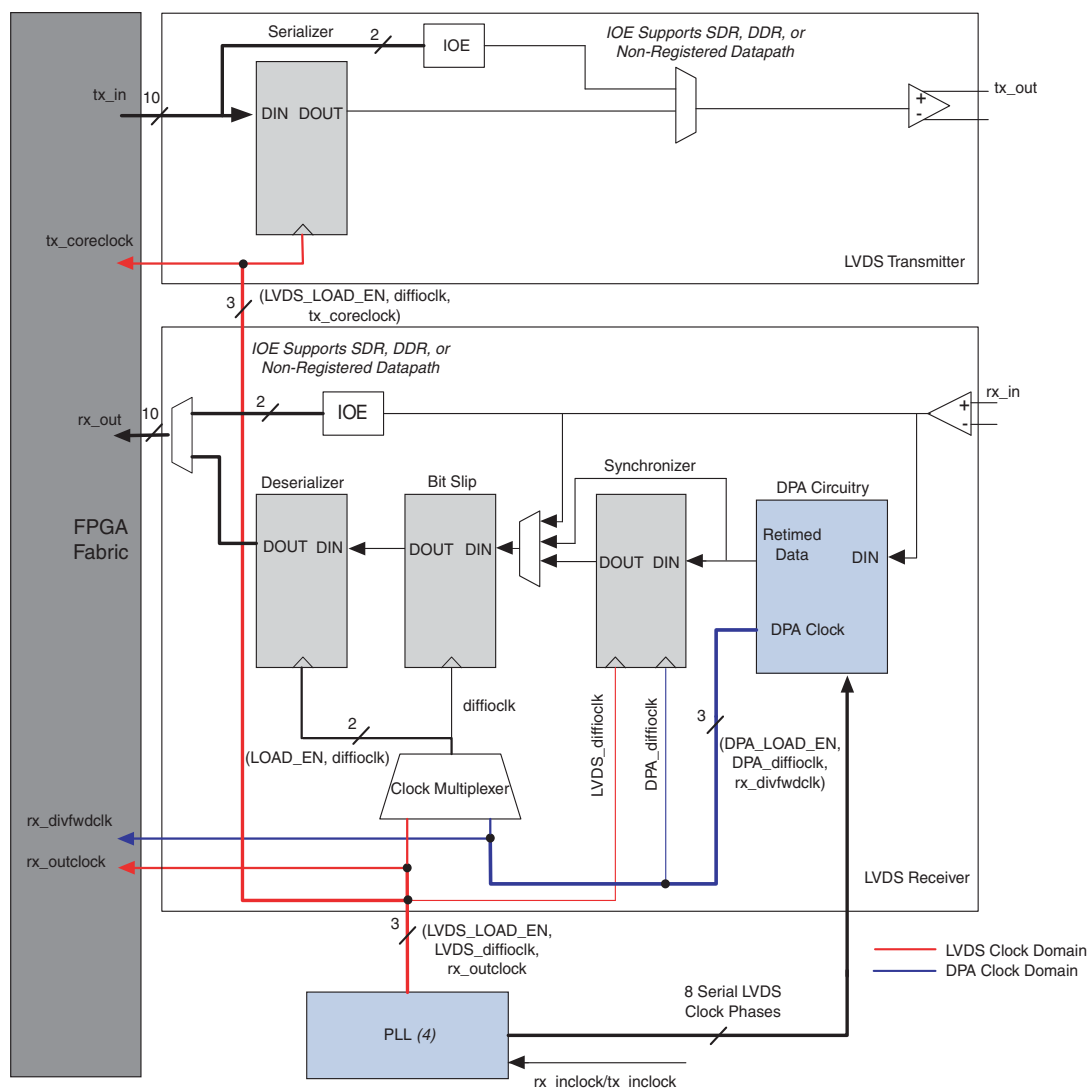
- (1) Rx = true LVDS input buffers without R_D OCT, eTx = emulated LVDS output buffers (either LVDS_E_1R or LVDS_E_3R).
- (2) The LVDS Rx and Tx channels are equally divided between the top and bottom sides of the device.
- (3) The LVDS channel count does not include dedicated clock input pins.

LVDS SERDES and DPA Block Diagram

The Arria II GX devices have dedicated SERDES and DPA circuitry for LVDS transmitters and receivers on the right side. The Arria II GZ devices have dedicated SERDES and DPA circuitry for LVDS transmitters and receivers on the row I/O banks.

Figure 8-3 shows the LVDS SERDES and DPA block diagram. This diagram shows the interface signals for the transmitter and receiver datapaths. For more information, refer to “Differential Transmitter” on page 8-8 and “Differential Receiver” on page 8-11.

Figure 8-3. LVDS SERDES and DPA Block Diagram (Note 1), (2), (3)



Notes to Figure 8-3:

- (1) This diagram shows a shared PLL between the transmitter and receiver. If the transmitter and receiver are not sharing the same PLL, two PLLs on the right side of the device are required.
- (2) In SDR and DDR modes, the data width is 1 and 2 bits, respectively.
- (3) The tx_in and rx_out ports have a maximum data width of 10 bits.
- (4) Arria II GX center/corner PLL or Arria II GZ left/right PLL.

Differential Transmitter

The Arria II transmitter has a dedicated circuitry to provide support for LVDS signaling. The dedicated circuitry consists of a differential buffer, a serializer, and PLLs that can be shared between the transmitter and receiver. The differential buffer can drive out LVDS, mini-LVDS, and RSDS signaling levels. The differential output buffer supports programmable pre-emphasis and programmable voltage output differential (V_{OD}) controls, and can drive out mini-LVDS and RSDS signaling levels. [Figure 8-4](#) is a block diagram of the LVDS transmitter.


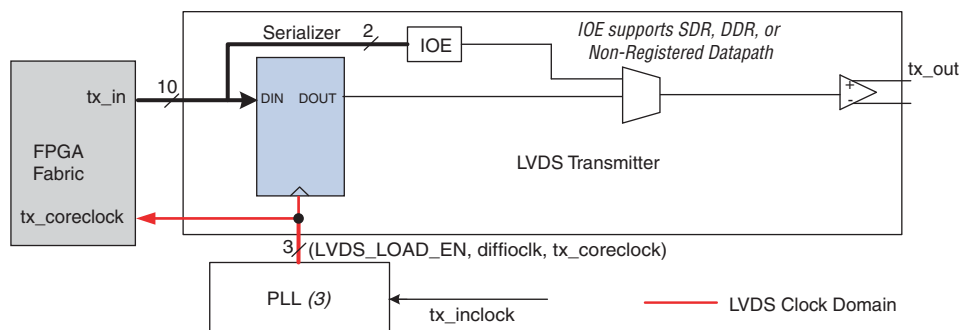
 When using emulated LVDS I/O standards at the differential transmitter, the SERDES circuitry must be implemented in logic cells but not hard SERDES.

Figure 8-4. LVDS Transmitter Block Diagram (Note 1), (2)



Notes to [Figure 8-4](#):

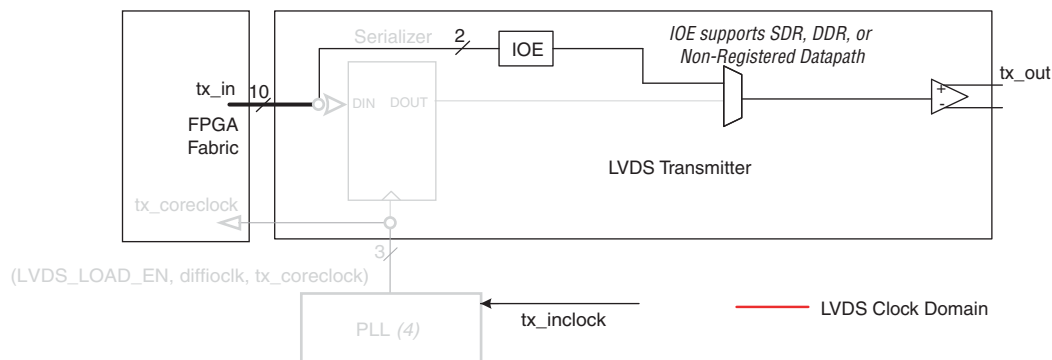
- (1) In SDR and DDR modes, the data width is 1 and 2 bits, respectively.
- (2) The `tx_in` port has a maximum data width of 10 bits.
- (3) Arria II GX center/corner PLL or Arria II GZ left/right PLL.

Serializer

The serializer takes parallel data from the FPGA fabric, clocks it into the parallel load registers, and serializes it using the shift registers before sending the data to the differential output buffer. The MSB of the parallel data is transmitted first. The parallel load and shift registers are clocked by the high-speed clock running at the serial data rate (`diffioclck`) and controlled by the load enable signal (`LVDS_LOAD_EN`) generated from the PLL. You can statically set the serialization factor to x4, x6, x7, x8, or x10 using the `ALTLVDS` megafunction. The load enable signal is derived from the serialization factor setting.

You can bypass the serializer to support DDR (x2) and SDR (x1) operations to achieve a serialization factor of 2 and 1, respectively. The I/O element (IOE) contains two data output registers that can each operate in either DDR or SDR mode. [Figure 8-5](#) shows the serializer bypass path.

Figure 8-5. Serializer Bypass Path (Note 1), (2), (3)



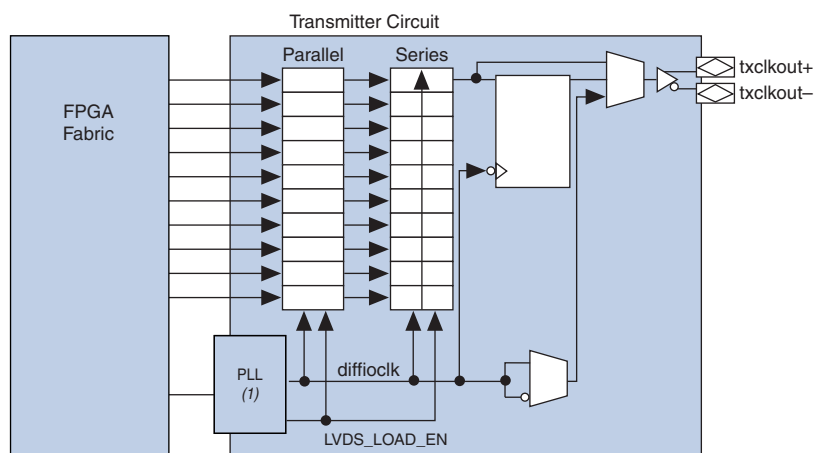
Notes to Figure 8-5:

- (1) All disabled blocks and signals are grayed out.
- (2) In DDR mode, tx_inclock clocks the IOE register. In SDR mode, data is directly passed through the IOE.
- (3) In SDR and DDR modes, the data width to the IOE is 1 and 2 bits, respectively.
- (4) Arria II GX center/corner PLL or Arria II GZ left/right PLL.

Differential applications often require specific clock-to-data alignments or a specific data rate to clock rate factors. You can configure any Arria II LVDS transmitter to generate a source-synchronous transmitter clock output. This flexibility allows the placement of the output clock near the data outputs to simplify board layout and reduce clock-to-data skew. The output clock can also be divided by a factor of 1, 2, 4, 6, 8, or 10, depending on the serialization factor. The phase of the clock in relation to the data can be set at 0° or 180° (edge or center aligned). The PLLs provide additional support for other phase shifts in 45° increments. These settings are made statically in the Quartus® II MegaWizard™ Plug-In Manager software.

Figure 8-6 shows the Arria II LVDS transmitter in clock output mode. In clock output mode, you can use an LVDS data channel as a clock output channel.

Figure 8-6. LVDS Transmitter in Clock Output Mode



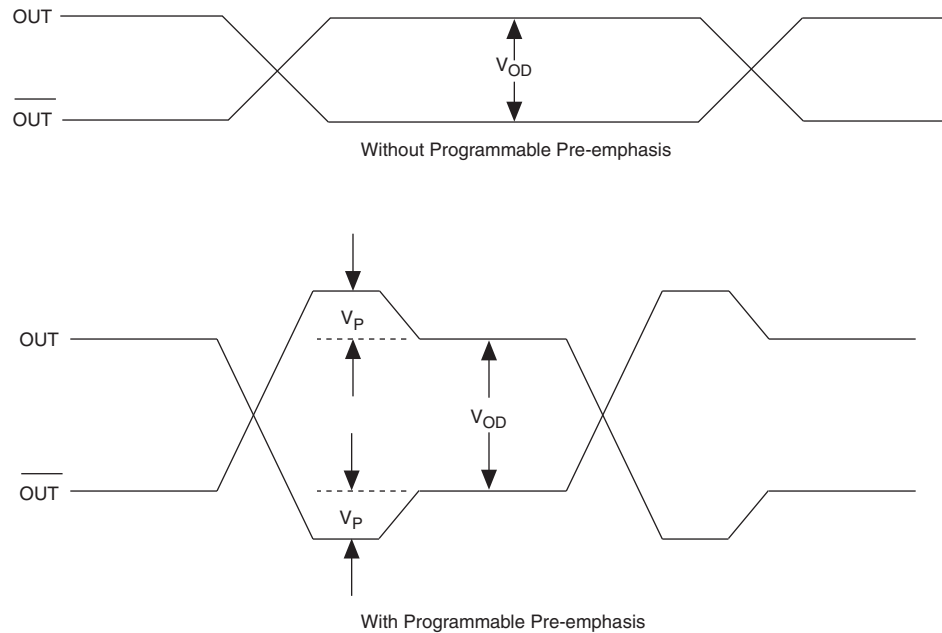
Note to Figure 8-6:

- (1) Arria II GX center/corner PLL or Arria II GZ left/right PLL.

Programmable Pre-Emphasis and Programmable V_{OD}

Pre-emphasis increases the amplitude of the high frequency component of the output signal, which helps to compensate for the frequency-dependent attenuation along the transmission line. Figure 8-7 shows the LVDS output single-ended waveform with and without pre-emphasis. The definition of V_{OD} is also shown.

Figure 8-7. LVDS Output Single-Ended Waveform with and without Programmable Pre-Emphasis (Note 1)



Note to Figure 8-7:

(1) V_P — voltage boost from pre-emphasis.

Pre-emphasis is an important feature for high-speed transmission. Without pre-emphasis, the output current is limited by the V_{OD} setting and the output impedance of the driver. At high frequency, the slew rate may not be fast enough to reach the full V_{OD} before the next edge, producing a pattern-dependent jitter. With pre-emphasis, the output current is boosted momentarily during switching to increase the output slew rate. The overshoot introduced by the extra current happens only during switching and does not ring, unlike the overshoot caused by signal reflection. This overshoot must not be included in the V_{OD} voltage.

Table 8-5 lists the assignment name and its possible values for programmable pre-emphasis in the Quartus II software Assignment Editor.

Table 8-5. Programmable Pre-Emphasis Settings in Quartus II Software Assignment Editor

Assignment Name	Assignment Value	
	Arria II GX Device	Arria II GZ Device
Programmable Pre-Emphasis	0 (off), 1 (default on)	0 (default zero), 1 (medium low), 2 (medium high), 3 (high)

You can statically assign the V_{OD} settings from the Assignment Editor. Table 8-6 lists the assignment name for programmable V_{OD} and its possible values in the Quartus II software Assignment Editor.

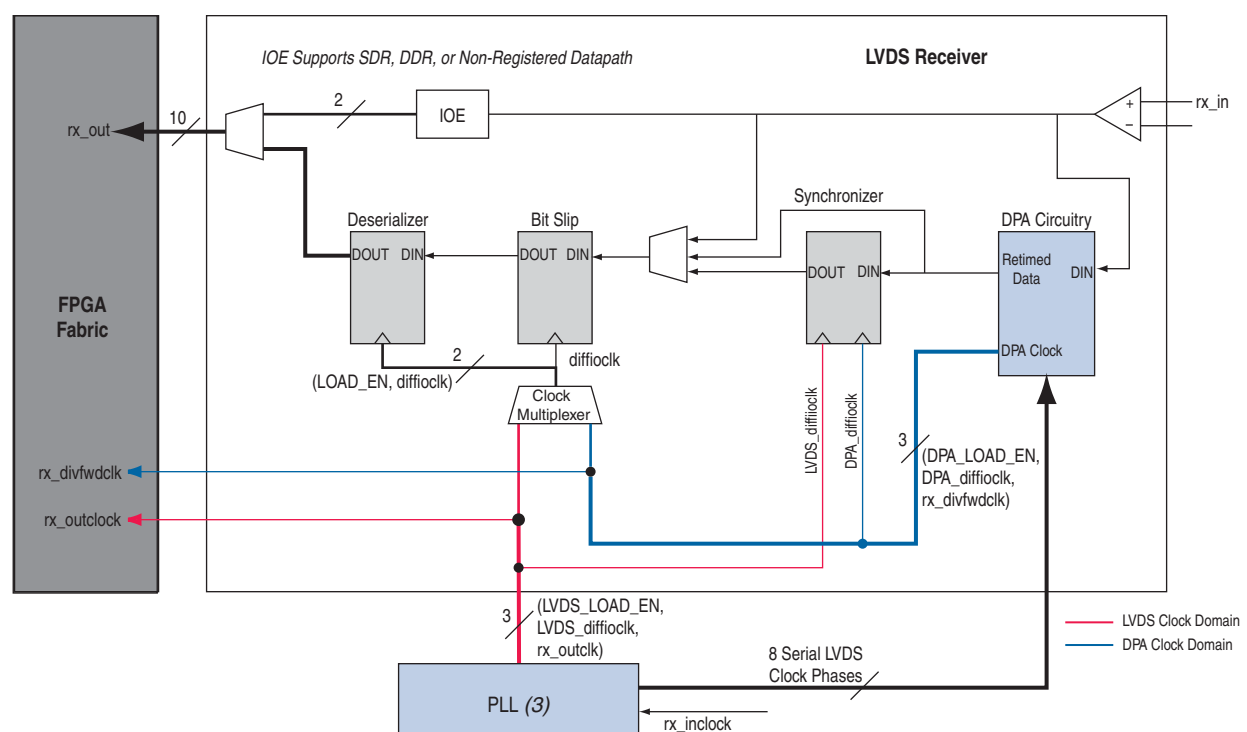
Table 8-6. Programmable V_{OD} Settings in Quartus II Software Assignment Editor

Assignment Name	Assignment Value	
	Arria II GX Device	Arria II GZ Device
Programmable Differential Output Voltage (V_{OD})	2	0, 1, 2, 3

Differential Receiver

The Arria II device family has a dedicated circuitry to receive high-speed differential signals in side or row I/Os. Figure 8-8 shows the hardware blocks of the Arria II receiver. The receiver has a differential buffer and PLLs that can be shared between the transmitter and receiver, a DPA block, a synchronizer, a data realignment block, and a deserializer. The differential buffer can receive LVDS signal levels, which are statically set in the Quartus II software Assignment Editor. Figure 8-8 shows a block diagram of an LVDS receiver in the right I/O bank.

Figure 8-8. LVDS Receiver Block Diagram (Note 1), (2)



Notes to Figure 8-8:

- (1) In SDR and DDR modes, the data width from the IOE is 1 and 2 bits, respectively.
- (2) The `rx_out` port has a maximum data width of 10 bits.
- (3) Arria II GX center/corner PLL or Arria II GZ left/right PLL.

The Arria II PLL receives the external reference clock input (`rx_inclock`) and generates eight different phases of the same clock. The DPA block chooses one of the eight clock phases from the center/corner PLL and aligns to the incoming data to maximize receiver skew margin. The synchronizer circuit is a 1-bit wide by 6-bit deep FIFO buffer that compensates for any phase difference between the DPA block and the deserializer. If necessary, the user-controlled data realignment circuitry inserts a single bit of latency in the serial bit stream to align to the word boundary. The deserializer converts the serial data to parallel data and sends the parallel data to the FPGA fabric.

The physical medium connecting the LVDS transmitter and the receiver channels may introduce skew between the serial data and the source synchronous clock. The instantaneous skew between each LVDS channel and the clock also varies with the jitter on the data and clock signals, as seen by the receiver.



Only non-DPA mode requires manual skew adjustment.

Arria II devices support the following receiver modes to overcome skew between the source-synchronous or reference clock and the received serial data:

- Non-DPA mode
- DPA mode
- Soft clock data recovery (CDR) mode



Dedicated SERDES and DPA circuitry only exist on the right side of the device. Top and bottom I/O banks only support non-DPA mode, in which the SERDES are implemented in the core logic.

Receiver Hardware Blocks

The differential receiver has the following hardware blocks:

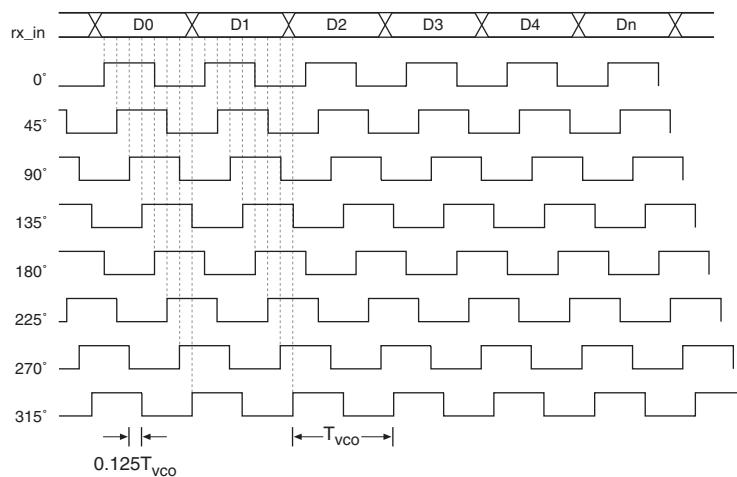
- “DPA” on page 8-12
- “Synchronizer” on page 8-13
- “Data Realignment Block (Bit Slip)” on page 8-14
- “Deserializer” on page 8-15

DPA

The DPA block takes in high-speed serial data from the differential input buffer and selects the optimal phase from one of the eight clock phases generated by the PLL to sample the data. The eight phases of the clock are equally divided, giving a 45° resolution. The maximum phase offset between the received data and the selected phase is 1/8 unit interval (UI), which is the maximum quantization error of the DPA block. The optimal clock phase selected by the DPA block (`DPA_diffclock`) is also used to write data into the FIFO buffer or to clock the SERDES for soft-CDR operation.

Figure 8-9 shows the possible phase relationships between the DPA clocks and the incoming serial data.

Figure 8-9. DPA Clock Phase to Serial Data Timing Relationship (Note 1)



Note to Figure 8-9:

(1) T_{vco} is defined as the PLL serial clock period.

The DPA block requires a training pattern and sequence of at least 256 repetitions. The training pattern is not fixed, so you can use any training pattern with at least one transition. An optional user controlled signal (`rx_dp11_hold`) freezes the DPA clock on its current phase when asserted. This signal is useful if you do not want the DPA circuitry to continuously adjust the phase after initial phase selection.

The DPA circuitry loses lock when it switches phases to maintain an optimal sampling phase. After it is locked, the DPA circuitry can lose the lock status under either of the following conditions:

- One phase change (adjacent to the current phase)
- Two phase changes in the same direction

An independent reset signal (`rx_reset`) is routed from the FPGA fabric to reset the DPA circuitry while in the user mode. The DPA circuitry must be retrained after reset.

Synchronizer

The synchronizer is a 1-bit wide and 6-bit deep FIFO buffer that compensates for the phase difference between `DPA_diffiocl` and the high-speed clock (`LVDS_diffiocl`) produced by the PLL. Because every DPA channel might have a different phase selected to sample the data, you need the FIFO buffer to synchronize the data to the high-speed LVDS clock domain. The synchronizer can only compensate for phase differences, not frequency differences between the data and the input reference clock of the receiver, and is automatically reset when the DPA circuitry first locks to the incoming data.

An optional signal (`rx_fifo_reset`) is available to the FPGA fabric to reset the synchronizer. Altera recommends using `rx_fifo_reset` to reset the synchronizer when the DPA signal is in a loss-of-lock condition and the data checker indicates corrupted received data.

Data Realignment Block (Bit Slip)

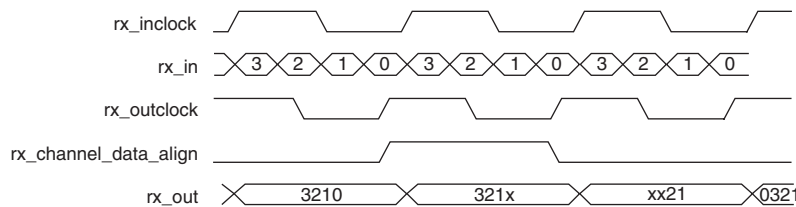
Skew in the transmitted data along with skew added by the link causes channel-to-channel skew on the received serial data streams. If you enabled the DPA block, the received data is captured with different clock phases on each channel and might cause the received data to be misaligned from channel to channel. To compensate for the channel-to-channel skew and establish the correct received word boundary at each channel, each receiver channel has a dedicated data realignment circuit that realigns the data by inserting bit latencies into the serial stream.

An optional signal (`rx_channel_data_align`) controls the bit insertion of each receiver independently controlled from the internal logic. The data slips one bit on the rising edge of `rx_channel_data_align`. The following are requirements for the `rx_channel_data_align` signal:

- An edge-triggered signal
- The minimum pulse width is one period of the parallel clock in the logic array
- The minimum low time between pulses is one period of the parallel clock
- Holding `rx_channel_data_align` does not result in extra slips
- Valid data is available two parallel clock cycles after the rising edge of the `rx_channel_data_align` signal

Figure 8-10 shows receiver output after a one bit-slip pulse with the deserialization factor set to 4.

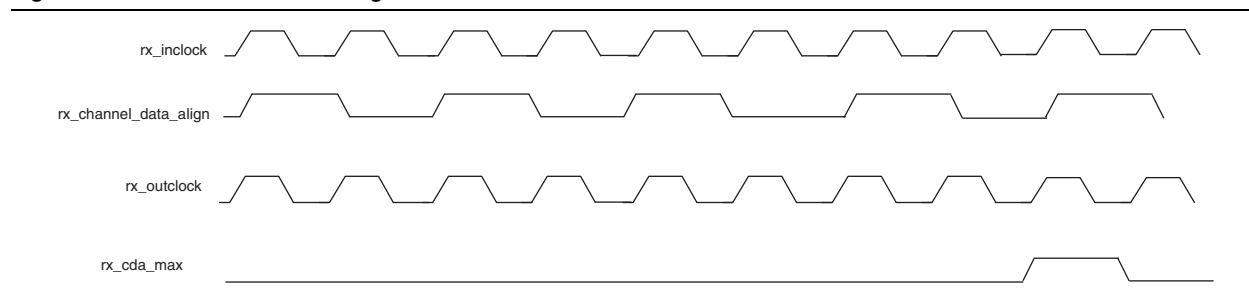
Figure 8-10. Data Realignment Timing



The data realignment circuit can have up to 11 bit-times of insertion before a rollover occurs. The programmable bit rollover point can be from 1 to 11 bit-times, independent of the deserialization factor. The programmable bit rollover point must be set to equal to or greater than the deserialization factor, allowing enough depth in the word alignment circuit to slip through a full word. You can set the value of the bit rollover point using the ALTLVDS megafunction. An optional status signal (`rx_cda_max`) is available to the FPGA fabric from each channel to indicate when the preset rollover point is reached.

Figure 8-11 shows a preset value of 4-bit times before rollover occurs. The rx_cda_max signal pulses for one rx_outclock cycle to indicate that rollover has occurred.

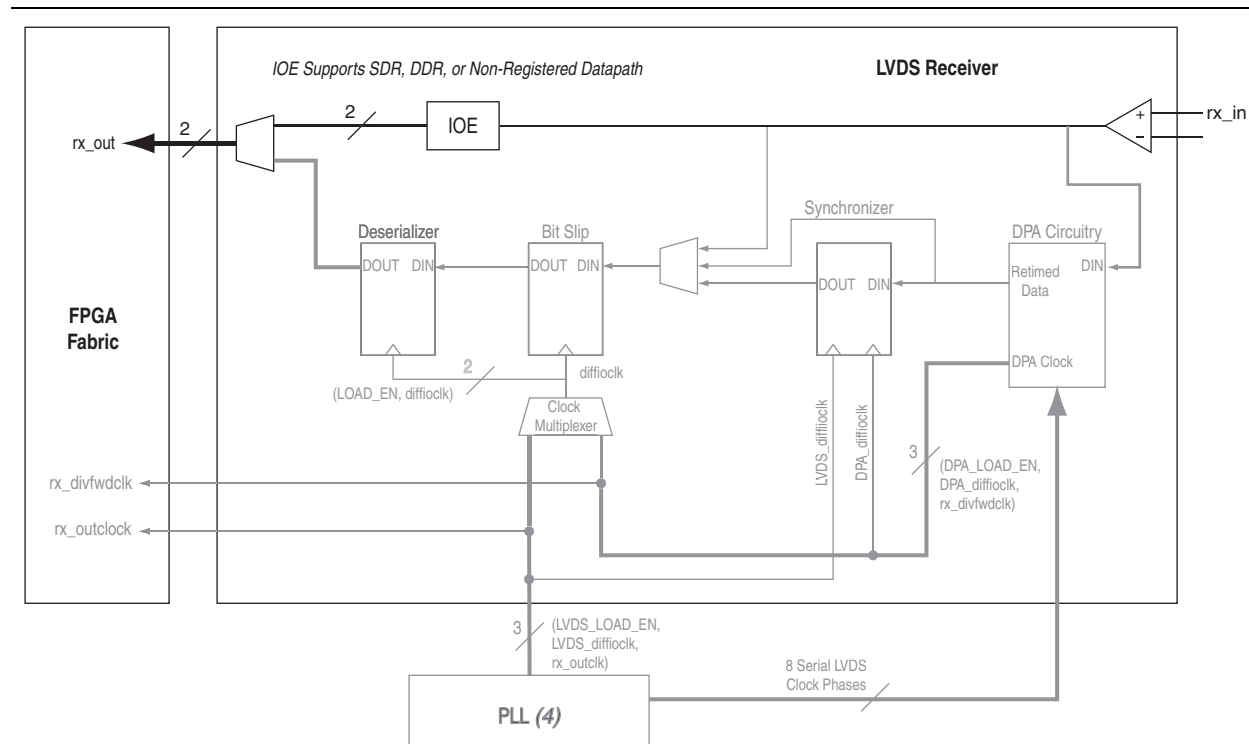
Figure 8-11. Receiver Data Re-Alignment Rollover



Deserializer

The deserializer, which includes shift registers and parallel load registers, converts the serial data from the bit slip to parallel data before sending the data to the FPGA fabric. The deserialization factor supported is 4, 6, 7, 8, or 10. You can bypass the deserializer to support DDR (x2) and SDR (x1) operations, as shown in Figure 8-12. You cannot use the DPA and data realignment circuit when the deserializer is bypassed. The IOE contains two data input registers that can operate in DDR or SDR mode.

Figure 8-12. Deserializer Bypass (Note 1), (2), (3)



Notes to Figure 8-12:

- (1) All disabled blocks and signals are grayed out.
- (2) In DDR mode, rx_inclock clocks the IOE register. In SDR mode, data is directly passed through the IOE.
- (3) In SDR and DDR modes, the data width from the IOE is 1 and 2 bits, respectively.
- (4) Arria II GX center/corner PLL or Arria II GZ left/right PLL.

Receiver Datapath Modes

Arria II devices support the following three receiver datapath modes:

- “Non-DPA”
- “DPA Mode”
- “Soft CDR Mode”

Non-DPA

Non-DPA mode allows you to statically select the optimal phase between the source-synchronous reference clock and the input serial data to compensate for any skew between the two signals. The reference clock must be a differential signal. [Figure 8-13](#) shows the non-DPA datapath block diagram. Input serial data is registered at the rising or falling edge of the `LVDS_diffioclk` clock produced by the PLL. You can select the **rising/falling edge** option using the `ALTLVDS` megafunction. Both data realignment and deserializer blocks are clocked by the `LVDS_diffioclk` clock.

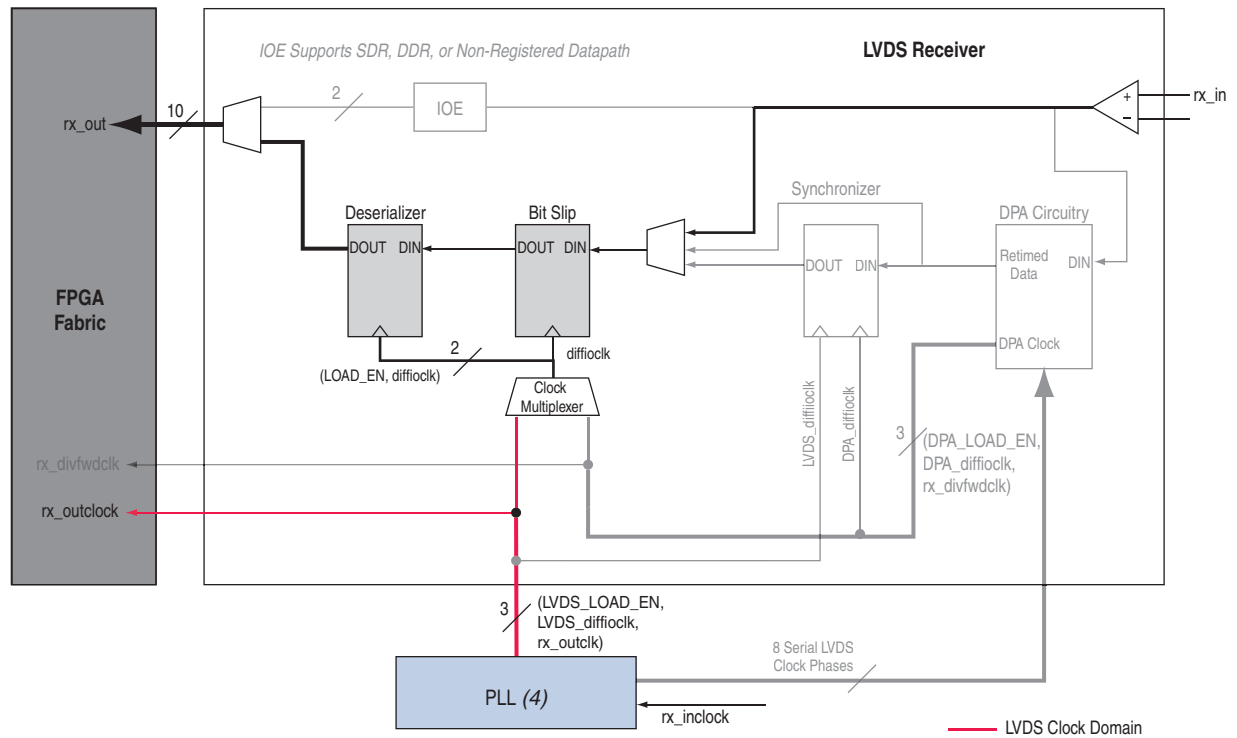
For Arria II GX devices, you must perform PCB trace compensation to adjust the trace length of each LVDS channel to improve channel-to-channel skew when interfacing with non-DPA receivers at data rate above 840 Mbps.

The Quartus II software Fitter Report panel reports the amount of delay you must add to each trace for the Arria II GX device. You can use the recommended trace delay numbers published under the LVDS Transmitter/Receiver Package Skew Compensation panel and manually compensate the skew on the PCB board trace to reduce channel-to-channel skew, thus meeting the timing budget between LVDS channels.



For more information about the LVDS Transmitter/Receiver Package Skew Compensation report panel, refer to the “Arria II GX LVDS Package Skew Compensation Report Panel” section in the *SERDES Transmitter/Receiver (ALTLVDS) Megafunction User Guide*.

Figure 8-13. Receiver Datapath in Non-DPA Mode (Note 1), (2), (3)



Notes to Figure 8-13:

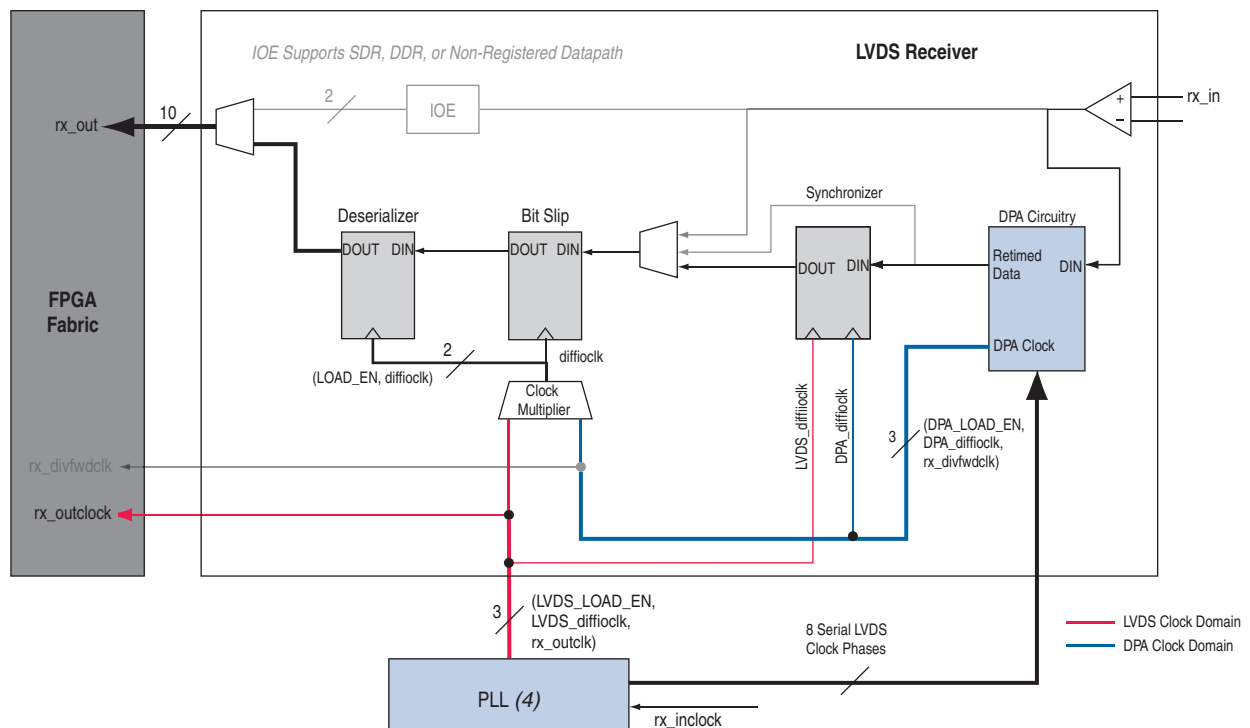
- (1) All disabled blocks and signals are grayed out.
- (2) In SDR and DDR modes, the data width from the IOE is 1 and 2 bits, respectively.
- (3) The **rx_out** port has a maximum data width of 10 bits.
- (4) Arria II GX center/corner PLL or Arria II GZ left/right PLL.

DPA Mode

In DPA mode, the DPA circuitry automatically chooses the optimal phase between the source-synchronous reference clock and the input serial data to compensate for the skew between the two signals. The reference clock must be a differential signal.

Figure 8-14 shows the DPA mode datapath. Use the `DPA_diffioclk` clock to write serial data into the synchronizer. Use the `LVDS_diffioclk` clock to read the serial data from the synchronizer. Use the same `LVDS_diffioclk` clock in the data realignment and deserializer blocks.

Figure 8-14. Receiver Datapath in DPA Mode (Note 1), (2), (3)



Notes to Figure 8-14:

- (1) All disabled blocks and signals are grayed out.
- (2) In SDR and DDR modes, the data width from the IOE is 1 and 2 bits, respectively.
- (3) The `rx_out` port has a maximum data width of 10 bits.
- (4) Arria II GX center/corner PLL or Arria II GZ left/right PLL.

Differential I/O Termination

The Arria II device family provides a 100- Ω R_D OCT option on each differential receiver channel for LVDS standards. OCT saves board space by eliminating the need to add external resistors on the board. You can enable OCT in the Quartus II software Assignment Editor.

For Arria II GX devices, OCT is supported in the top, right, and bottom I/O banks. Arria II GX clock input pins (CLK[4 . . 15]) do not support OCT. For Arria II GZ devices, R_D OCT is supported on all row I/O pins and dedicated clock input pins (CLK[0, 2, 9, 11]). It is not supported for column I/O pins and dedicated clock input pins (CLK[1, 3, 8, 10]).

Figure 8-16 shows LVDS input OCT.

Figure 8-16. LVDS Input Buffer I/O R_D OCT

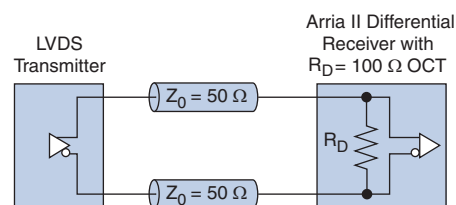


Table 8-7 lists the assignment name and its value for differential input OCT in the Quartus II software Assignment Editor.

Table 8-7. Differential Input OCT in Quartus II Software Assignment Editor


Assignment Name	Assignment Value
Input Termination (Accepts wildcards/groups)	Differential

 For more information, refer to *I/O Features in Arria II Devices* chapter.

PLLs

Arria II GX devices contain up to six PLLs with up to four center and corner PLLs located on the right side of the device. Use the center/corner PLL on the right side of the device to generate parallel clocks (`rx_outclock` and `tx_outclock`) and high-speed clocks (`diffioclk`) for the SERDES and DPA circuitry. [Figure 8-1 on page 8-3](#) shows the locations of the PLLs for Arria II GX devices. Clock switchover and dynamic reconfiguration are allowed using the center/corner PLLs in high-speed differential I/O support mode.

Arria II GZ devices contain up to four left and right PLLs with up to two PLLs located on the left side and two on the right side of the device. The left PLLs can support high-speed differential I/O banks on the left side; the right PLLs can support high-speed differential I/O banks on the right side of the device. The high-speed differential I/O receiver and transmitter channels use these left and right PLLs to generate the parallel clocks (`rx_outclock` and `tx_outclock`) and high-speed clocks (`diffioclk`). [Figure 8-2 on page 8-4](#) shows the locations of the left and right PLLs for Arria II GZ devices. The PLL VCO operates at the clock frequency of the data rate. Clock switchover and dynamic reconfiguration are allowed using the left and right PLL in high-speed differential I/O support mode.

 For more information about PLLs, refer to the [Clock Network and PLLs in Arria II Devices](#) chapter.

LVDS and DPA Clock Networks

Arria II GX devices only have LVDS and DPA clock networks on the right side of the device. The center/corner PLLs feed into the differential transmitter and receiver channels through the LVDS and DPA clock networks. [Figure 8-17](#) and [Figure 8-18](#) show the LVDS clock tree for family members without center PLLs and with center PLLs, respectively. The center PLLs can drive the LVDS clock tree above and below them. In Arria II GX devices with or without center PLLs, the corner PLLs can drive both top and bottom LVDS clock tree.

Figure 8-17. LVDS and DPA Clock Networks in the Arria II GX Devices without Center PLLs

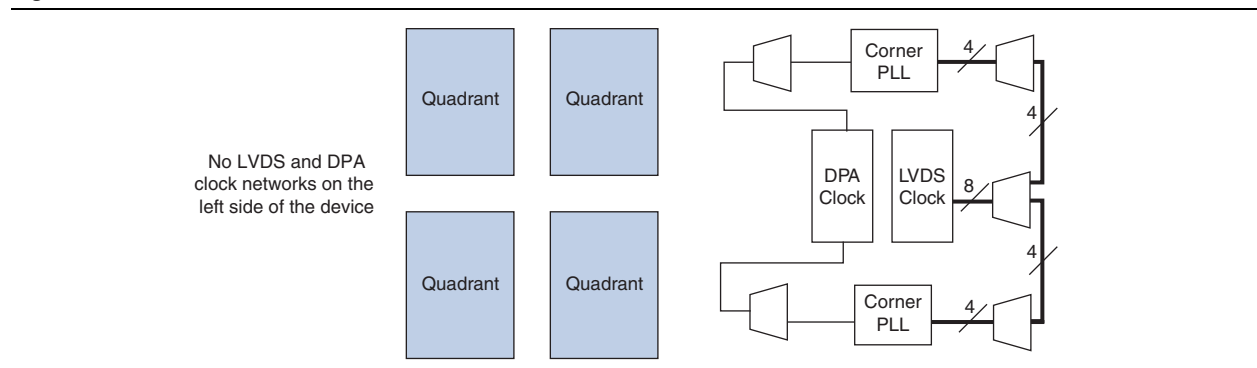
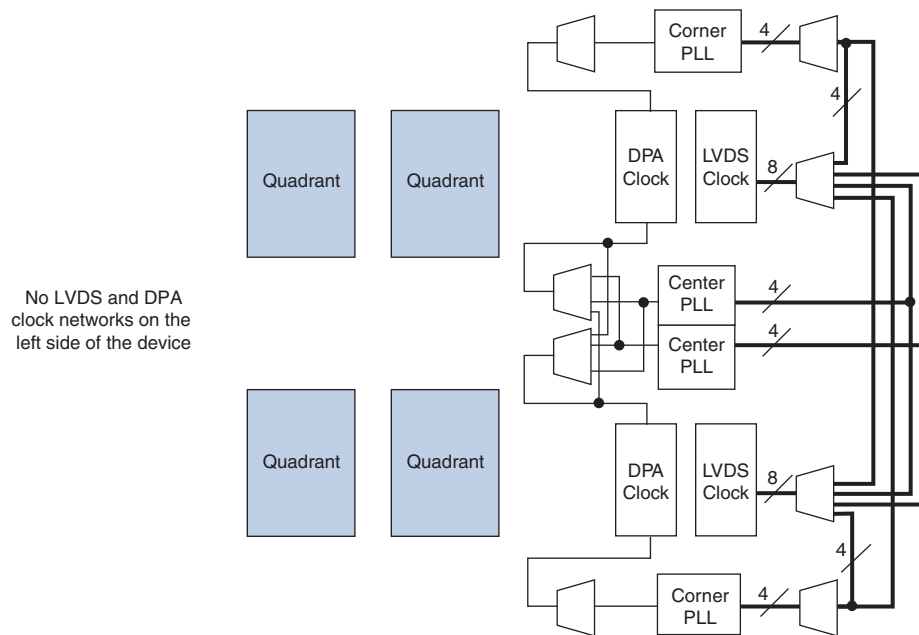
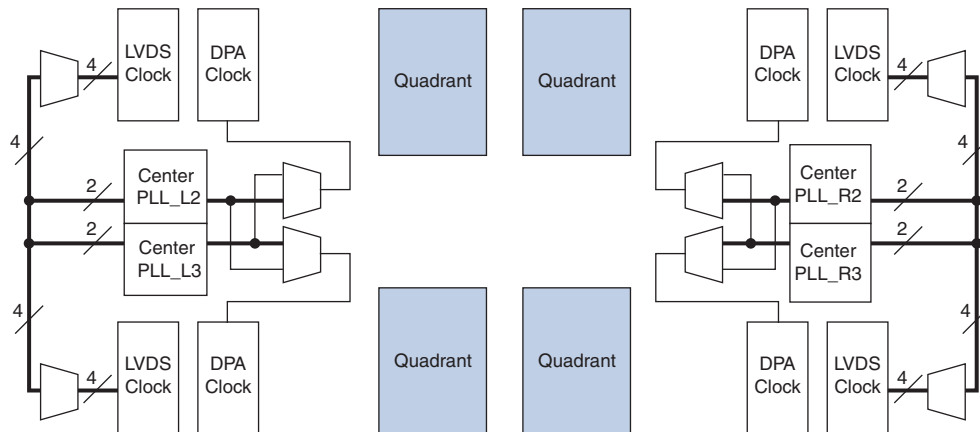


Figure 8-18. LVDS and DPA Clock Networks in the Arria II GX Devices with Center PLLs

Arria II GZ devices have left and right PLLs that feed into the differential transmitter and receive channels through the LVDS and DPA clock network. The center left and right PLLs can clock the transmitter and receive channels above and below them.

Figure 8-19 shows center PLL clocking in Arria II GZ devices.

Figure 8-19. LVDS/DPA Clocks in the Arria II GZ Devices with Center PLLs

For more information about Arria II devices PLL clocking restrictions, refer to [“Differential Pin Placement Guidelines”](#) on page 8-27.

Source-Synchronous Timing Budget

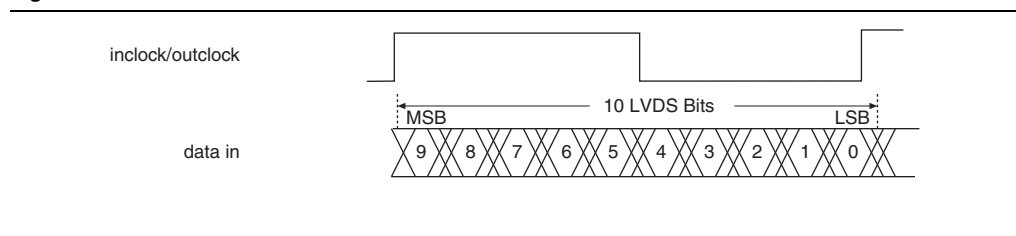
This section describes the timing budget, waveforms, and specifications for source-synchronous signaling in Arria II devices. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques. Therefore, it is important to understand how to analyze timing for high-speed differential signals. This section defines the source-synchronous differential data orientation timing parameters, timing budget definitions, and how to use these timing parameters to determine your design's maximum performance.

Differential Data Orientation

There is a set relationship between an external clock and the incoming data. For operation at 1 Gbps and a serialization factor of 10, the external clock is multiplied by 10. You can set the phase-alignment in the PLL to coincide with the sampling window of each data bit. The data is sampled on the falling edge of the multiplied clock.

Figure 8–20 shows the data bit orientation of x10 mode.

Figure 8–20. Bit Orientation

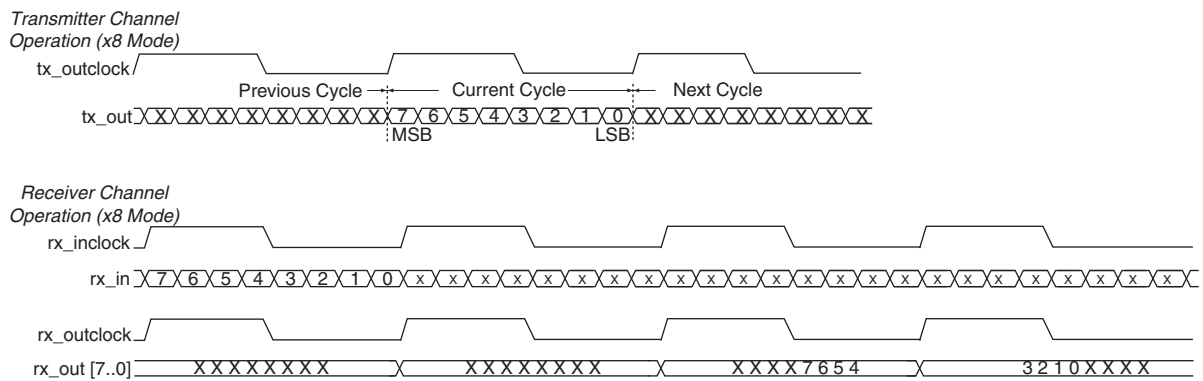


Differential I/O Bit Position

Data synchronization is necessary for successful data transmission at high frequencies. Figure 8–21 shows data bit orientation for a channel operation. These figures are based on the following:

- serialization factor equals clock multiplication factor
- edge alignment is selected for phase alignment
- implemented in hard SERDES

For other serialization factors, use the Quartus II software tools to find the bit position in the word. The bit positions after deserialization are listed in Table 8–8.

Figure 8-21. Bit Order and Word Boundary for One Differential Channel (Note 1)**Note to Figure 8-21:**

(1) These waveforms are only functional waveforms and are not intended to convey timing information.

Table 8-8 lists the conventions for differential bit naming for 18 differential channels. The MSB and LSB positions increase with the number of channels used in a system.

Table 8-8. Differential Bit Naming

Receiver Channel Data Number	Internal 8-Bit Parallel Data	
	MSB Position	LSB Position
1	7	0
2	15	8
3	23	16
4	31	24
5	39	32
6	47	40
7	55	48
8	63	56
9	71	64
10	79	72
11	87	80
12	95	88
13	103	96
14	111	104
15	119	112
16	127	120
17	135	128
18	143	136

Transmitter Channel-to-Channel Skew

Transmitter channel-to-channel skew (TCCS) is an important parameter based on the Arria II transmitter in a source synchronous differential interface. This parameter is used in receiver skew margin calculation.

TCCS is the difference between the fastest and slowest data output transitions, including the TCO variation and clock skew. For LVDS transmitters, the TimeQuest Timing Analyzer provides a TCCS report, which shows TCCS values for serial output ports.



You can get the TCCS value from the TCCS report (report_TCCS) in the Quartus II compilation report under the TimeQuest analyzer or from the *Arria II Device Data Sheet* chapter.

Receiver Skew Margin for Non-DPA Mode

Changes in system environment, such as temperature, media (cable, connector, or PCB), and loading, effect the receiver's setup and hold times; internal skew affects the sampling ability of the receiver.

Different modes of LVDS receivers use different specifications, which can help in deciding the ability to sample the received serial data correctly. In DPA mode, use DPA jitter tolerance instead of receiver skew margin (RSKM).

In non-DPA mode, use RSKM, TCCS, and sampling window (SW) specifications for high-speed source-synchronous differential signals in the receiver datapath. The relationship between RSKM, TCCS, and SW is expressed by the RSKM equation shown in [Equation 8-1](#):

Equation 8-1.

$$\text{RSKM} = \frac{\text{TUI} - \text{SW} - \text{TCCS}}{2}$$

Where:

- TUI—the time period of the serial data.
- RSKM—the timing margin between the receiver's clock input and the data input SW.
- SW—the period of time that the input data must be stable to ensure that the data is successfully sampled by the LVDS receiver. The sampling window is the device property and varies with the device speed grade.
- TCCS—the difference between the fastest and slowest data output transitions, including the t_{CO} variation and clock skew.

You must calculate the RSKM value to decide whether or not the data can be sampled properly by the LVDS receiver with the given data rate and device. A positive RSKM value indicates the LVDS receiver can sample the data properly; a negative RSKM indicates the receiver cannot sample the data properly.

Differential Pin Placement Guidelines

To ensure proper high-speed operation, differential pin placement guidelines are established. The Quartus II Compiler automatically checks that these guidelines are followed and issues an error message if they are not adhered to.



DPA-enabled differential channels refer to DPA mode or soft CDR mode; DPA-disabled channels refer to non-DPA mode.

DPA-Enabled Channels and Single-Ended I/Os

When single-ended I/Os and LVDS I/Os share the same I/O bank, the placement of single-ended I/O pins with respect to LVDS I/O pins is restricted. The constraints on single-ended I/Os placement with respect to DPA-enabled or DPA-disabled LVDS I/Os are the same.

- Single-ended I/Os are allowed in the same I/O bank, if the single-ended I/O standard uses the same V_{CCIO} as the DPA-enabled differential I/O bank.
- Single-ended inputs can be in the same logic array block (LAB) row as a differential channel using the SERDES circuitry.
- Double data rate I/O (DDIO) can be placed within the same LAB row as a SERDES differential channel but half rate DDIO or single data rate (SDR) output pins cannot be placed within the same LAB row as a receiver SERDES differential channel. The input register must be implemented within the FPGA fabric logic.

Guidelines for DPA-Enabled Differential Channels

When you use DPA-enabled channels, you must adhere to the guidelines listed in the following sections.

DPA-Enabled Channel Driving Distance

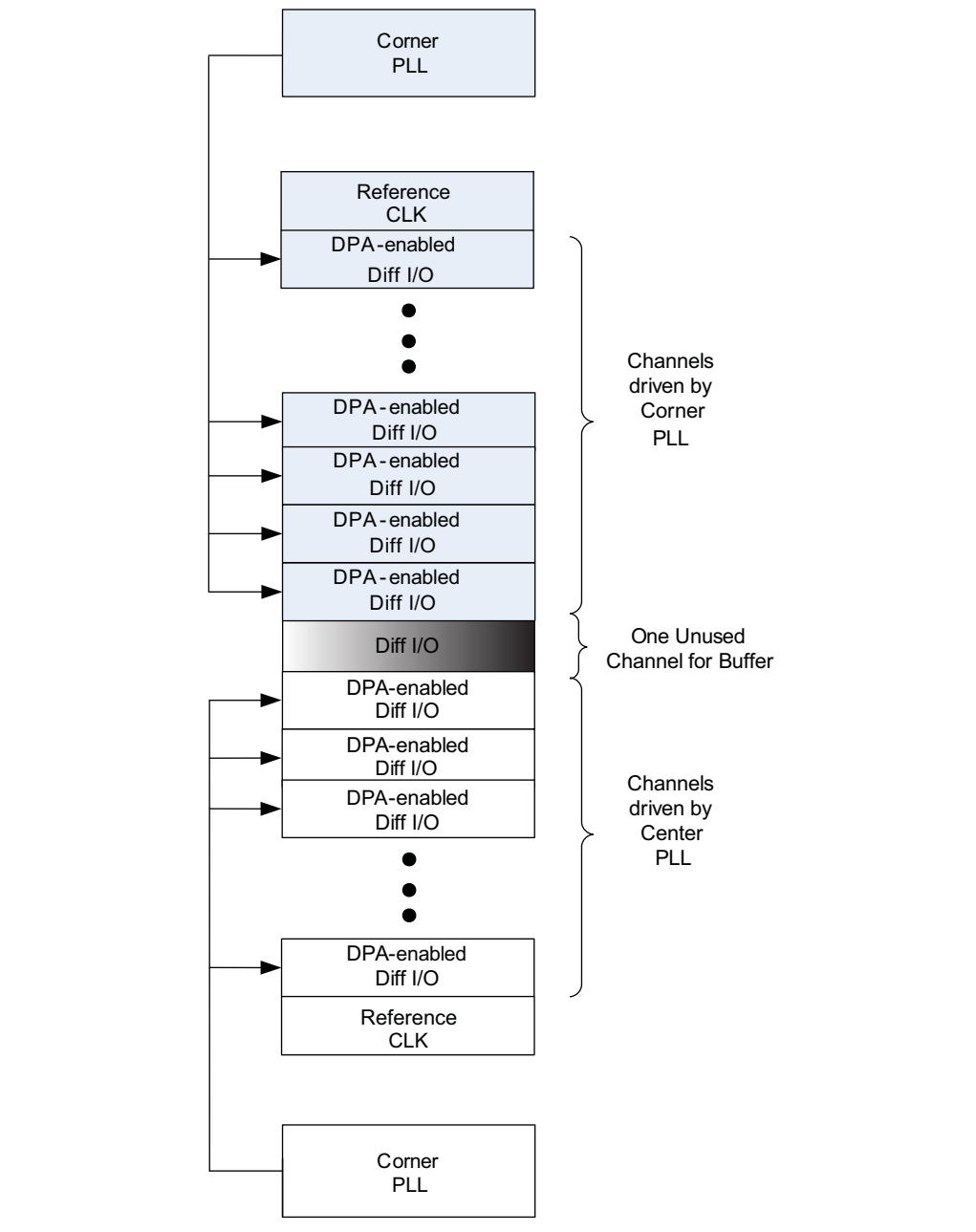
If the number of DPA-enabled channels driven by each center or corner PLL exceeds 25 LAB rows, Altera recommends implementing data realignment (bit slip) circuitry for all the DPA channels.

Using Center and Corner Left and Right PLLs in Arria II GX Devices

If the DPA-enabled channels in a bank are being driven by two PLLs, where the corner PLL is driving one group and the center PLL is driving another group, there must be at least one row of separation between the two groups of DPA-enabled channels, as shown in [Figure 8-23](#). This separation prevents noise mixing because the two groups can operate at independent frequencies.


No separation is necessary if a single PLL is driving both the DPA-enabled channels and DPA-disabled channels.

Figure 8-23. Center and Corner PLLs Driving DPA-Enabled Differential I/Os in the Same Bank



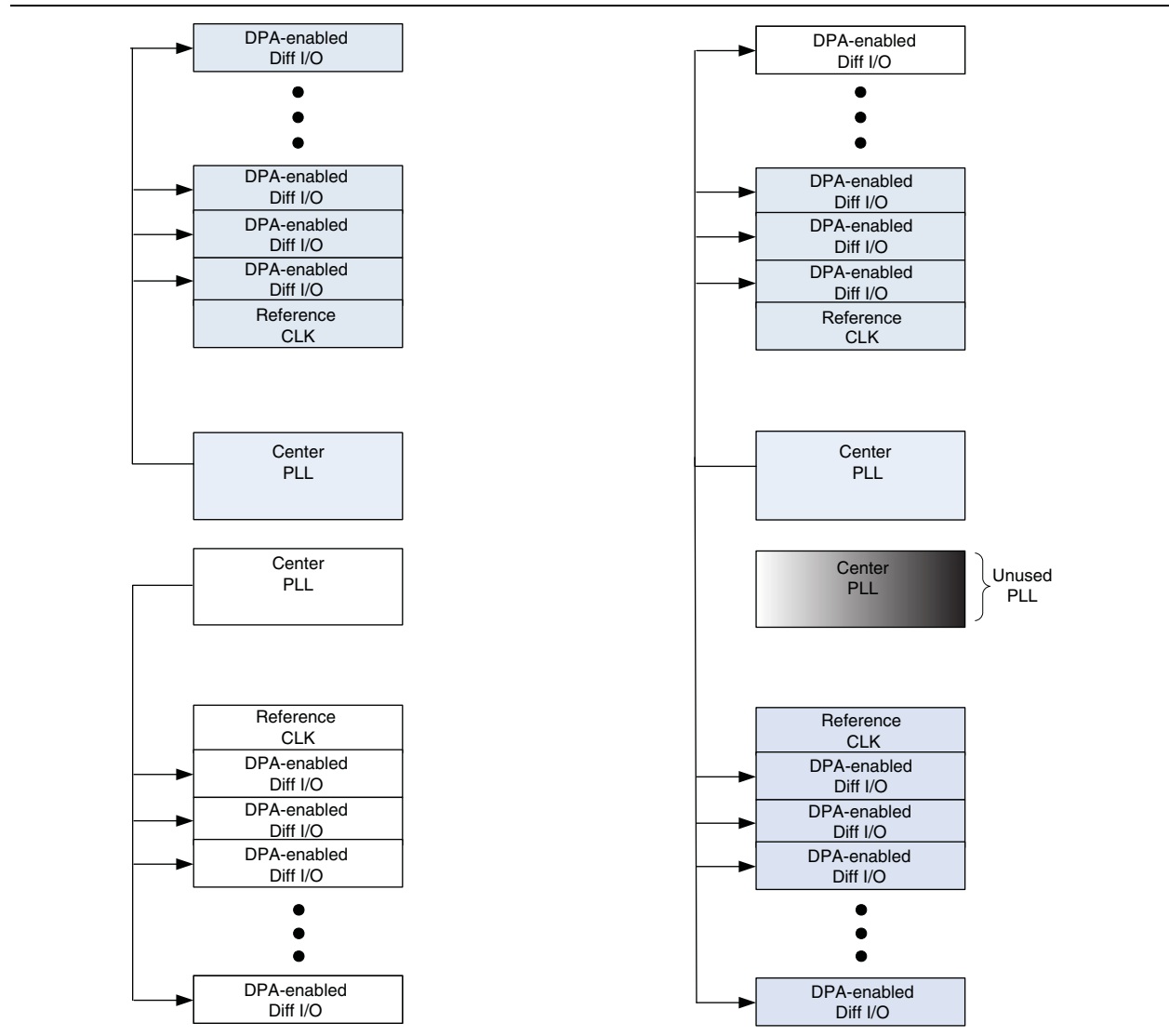
Using Both Center PLLs

You can use center PLLs to drive DPA-enabled channels simultaneously, if they drive these channels in their adjacent banks only, as shown in [Figure 8-23](#).

 Center PLLs are available at the right I/O banks of Arria II GX devices and the right and left I/O banks of Arria II GZ devices.

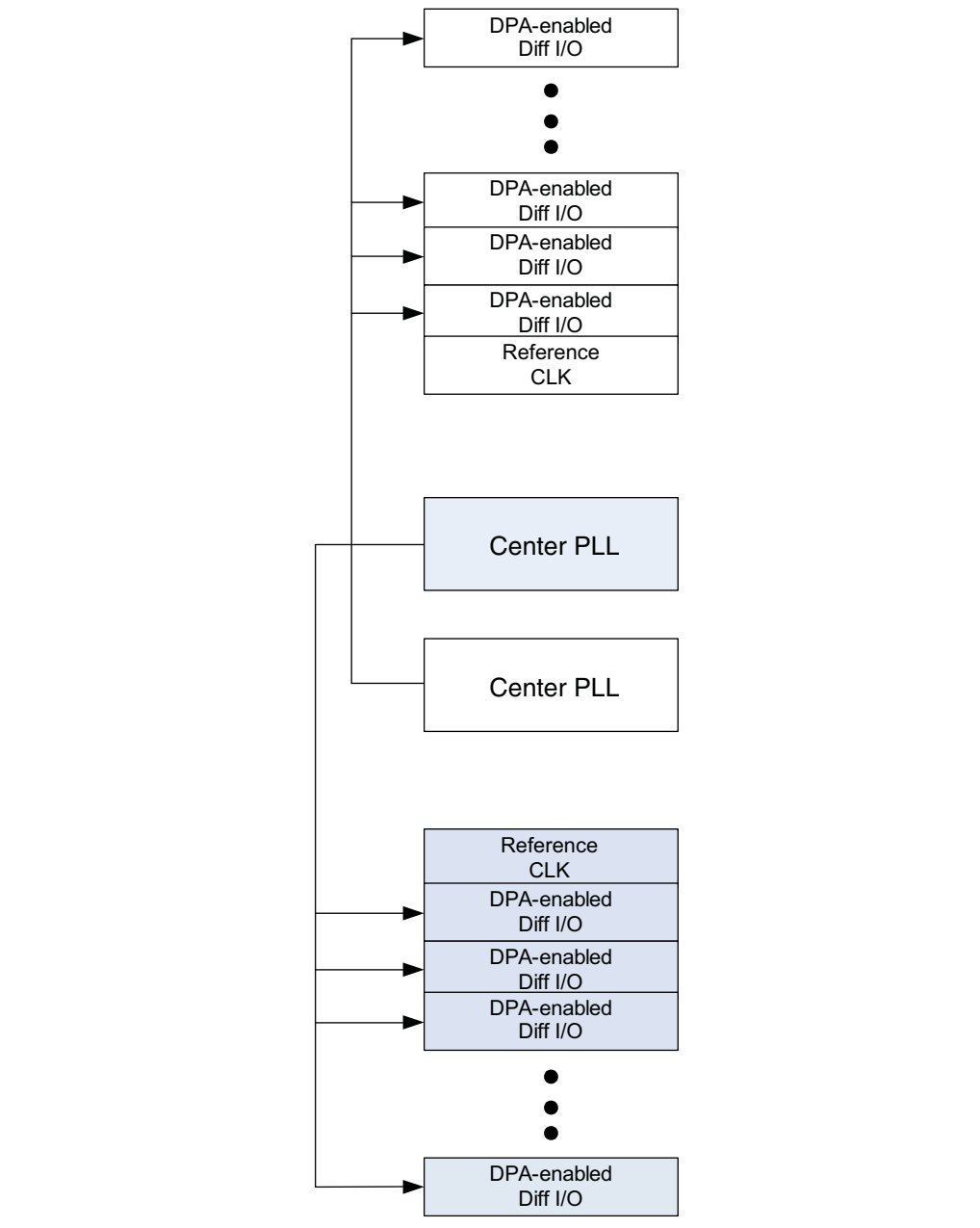
If one of the center PLLs drives the DPA-enabled channels in the upper and lower I/O banks, you cannot use the other center PLL for DPA-enabled channels, as shown in [Figure 8-24](#).

Figure 8-24. Center PLLs Driving DPA-Enabled Differential I/Os



If the upper center PLL drives DPA-enabled channels in the lower I/O bank, the lower center PLL cannot drive DPA-enabled channels in the upper I/O bank, and vice versa. In other words, the center PLLs cannot drive cross-banks simultaneously, as shown in Figure 8-25.

Figure 8-25. Invalid Placement of DPA-Disabled Differential I/Os Driven by Both Center PLLs



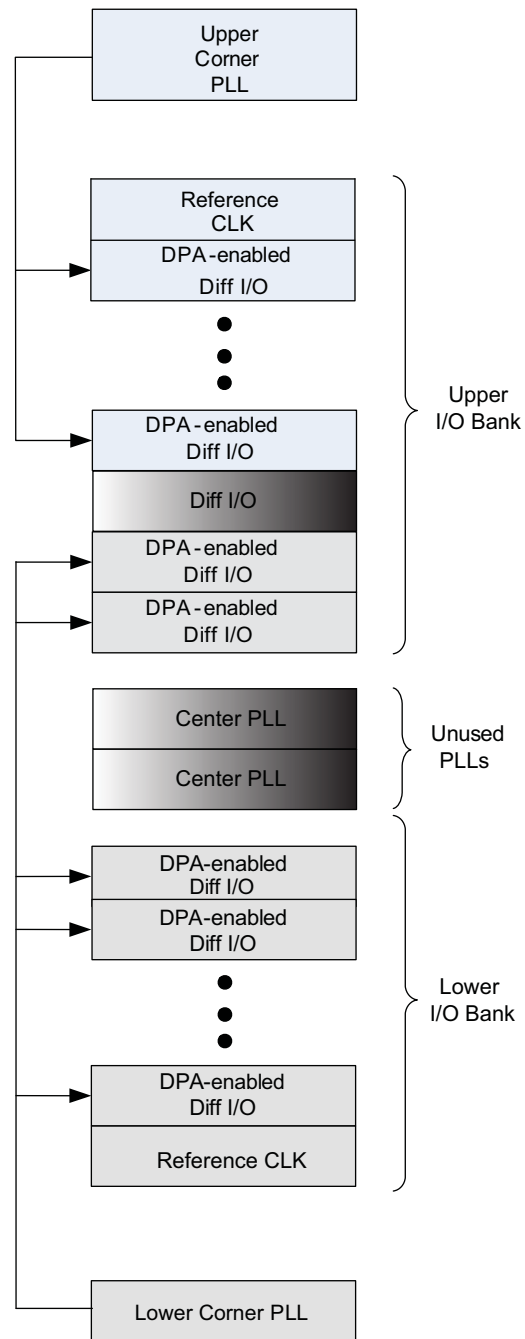
Using Both Corner PLLs in Arria II GX Devices

You can use both corner PLLs to drive DPA-enabled channels simultaneously, if they drive the channels in their adjacent banks only. There must be at least one row of separation between the two groups of DPA-enabled channels.

If one of the corner PLLs drives DPA-enabled channels in the upper and lower I/O banks, you cannot use the center PLLs. You can use the other corner PLL to drive DPA-enabled channels in their adjacent bank only. There must be at least one row of separation between the two groups of DPA-enabled channels.

If the upper corner PLL drives DPA-enabled channels in the lower I/O bank, the lower corner PLL cannot drive DPA-enabled channels in the upper I/O bank, and vice versa. In other words, the corner PLLs cannot drive cross-banks simultaneously, as shown in [Figure 8-26](#).

Figure 8-26. Corner PLLs Driving DPA-Enabled Differential I/Os



Guidelines for DPA-Disabled Differential Channels

When you use DPA-disabled channels, you must adhere to the guidelines in the following sections.

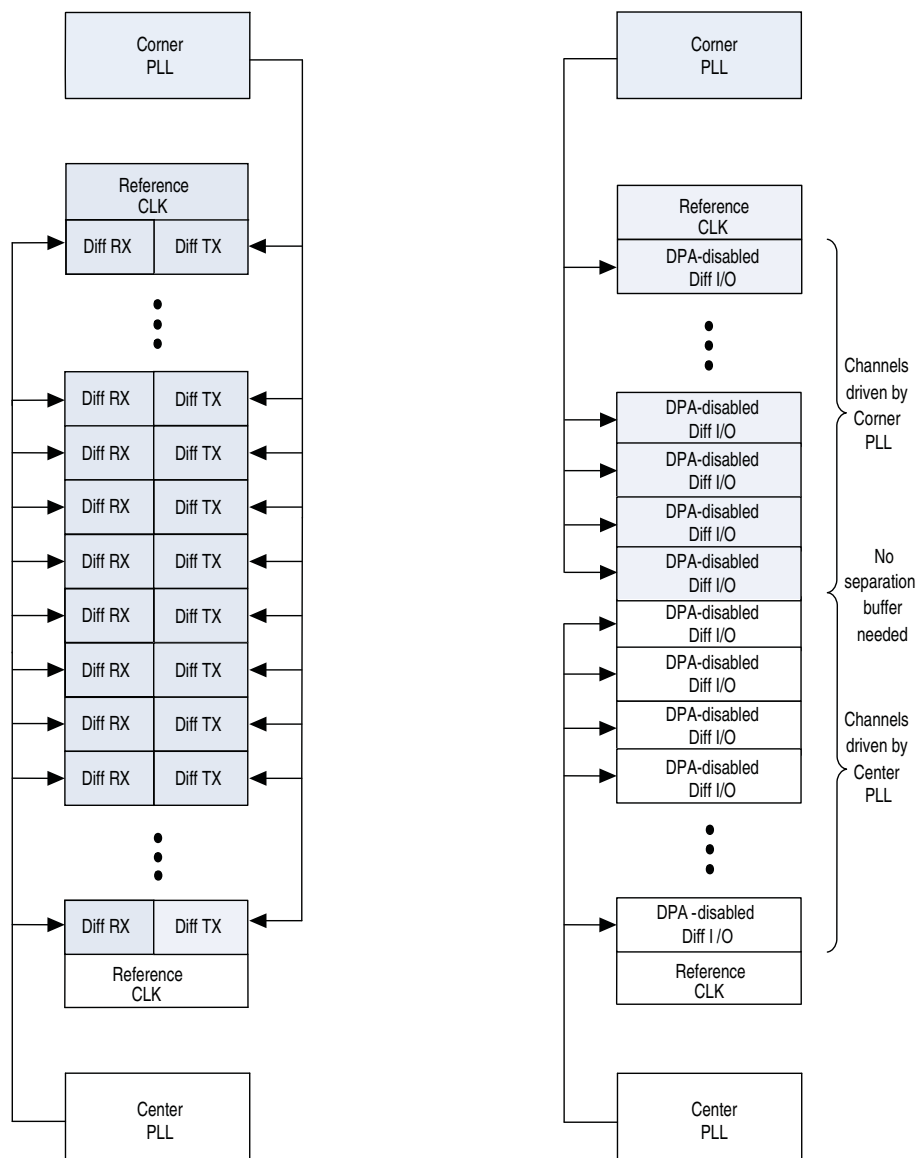
DPA-Disabled Channel Driving Distance

Each PLL can drive all the DPA-disabled channels in the entire bank.

Using Corner and Center PLLs in Arria II GX Devices

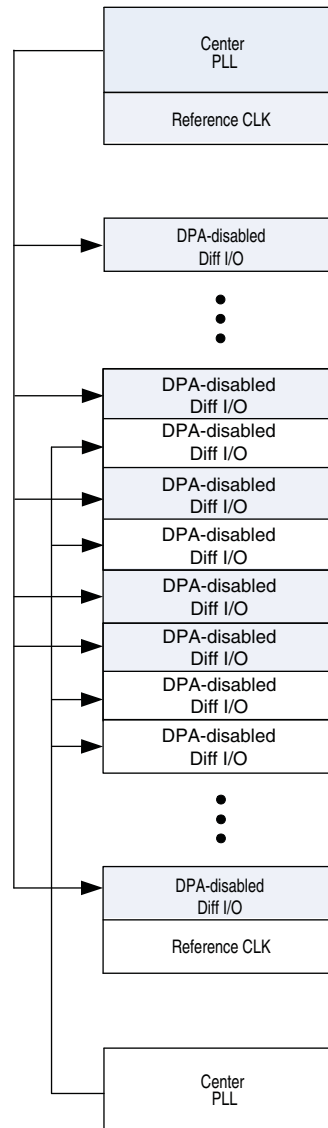
You can use a corner PLL to drive all transmitter channels and you can use a center PLL to drive all DPA-disabled receiver channels in the same I/O bank. In other words, you can drive a transmitter channel and a receiver channel in the same LAB row by two different PLLs, as shown in Figure 8-27.

Figure 8-27. Corner and Center PLLs Driving DPA-Disabled Differential I/Os in the Same Bank



A corner PLL and a center PLL can drive duplex channels in the same I/O bank, if the channels driven by each PLL are not interleaved. No separation is necessary between the group of channels driven by the corner and center left and right PLLs. Refer to [Figure 8-27](#) and [Figure 8-28](#).

Figure 8-28. Invalid Placement of DPA-Disabled Differential I/Os Due to Interleaving of Channels Driven by the Corner and Center PLLs



Using Both Center PLLs

You can use both center PLLs simultaneously to drive DPA-disabled channels on upper and lower I/O banks. Unlike DPA-enabled channels, the center PLLs can drive DPA-disabled channels cross-banks. For example, the upper center PLL can drive the lower I/O bank at the same time the lower center PLL is driving the upper I/O bank, and vice versa, as shown in [Figure 8-29](#).


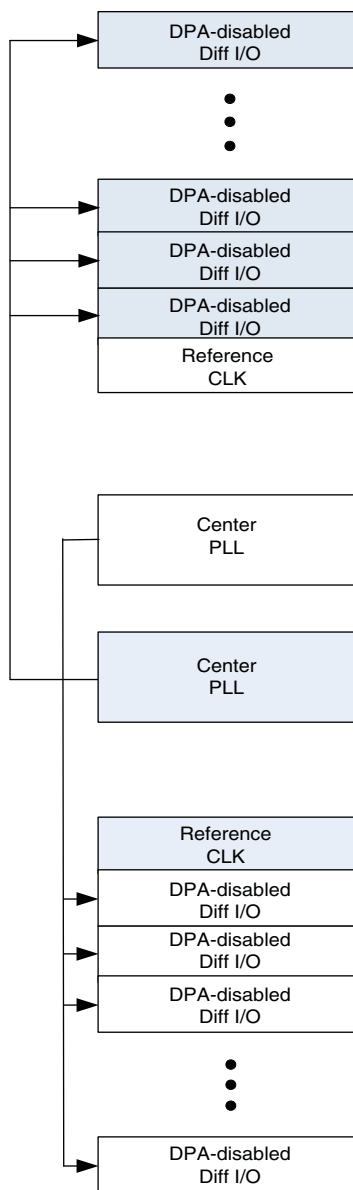
 Center PLLs are available at the right I/O banks of Arria II GX devices and the right and left I/O banks of Arria II GZ devices.

Figure 8-29. Both Center PLLs Driving Cross-Bank DPA-Disabled Channels Simultaneously



Using Both Corner PLLs in Arria II GX Devices

You can use both corner PLLs to drive DPA-disabled channels simultaneously. Both corner PLLs can drive cross-banks.



You can use a corner PLL to drive all the transmitter channels and you can use the other corner PLL to drive all DPA-disabled receiver channels in the same I/O bank.

Both corner PLLs can drive duplex channels in the same I/O bank if the channels driven by each PLL are not interleaved. No separation is necessary between the group of channels driven by both corner PLLs.

Setting Up an LVDS Transmitter or Receiver Channel

The ALTLVDS megafunction offers you the ease of setting up an LVDS transmitter or receiver channel. You can control the settings of SERDES and DPA circuitry in the ALTLVDS megafunction. When you instantiate an ALTLVDS megafunction, the PLL is instantiated automatically and you can set the parameters of the PLL. This megafunction simplifies the clocking setup for the LVDS transmitter or receiver channels. However, the drawback is reduced flexibility when using the PLL.

The ALTLVDS megafunction provides an option for implementing the LVDS transmitter or receiver interfaces with external PLLs. With this option enabled, you can control the PLL settings, such as dynamically reconfiguring the PLLs to support different data rates, dynamic phase shift, and other settings. You also must instantiate an ALTPLL megafunction to generate the various clock and load enable signals.

-  For more information about how to control the PLL, SERDES, and DPA block settings, and detailed descriptions of the LVDS transmitter and receiver interface signals, refer to the *SERDES Transmitter/Receiver (ALTLVDS) Megafunction User Guide*.
-  For more information about the ALTPLL megafunction, refer to the *Phase Locked-Loops (ALTPLL) Megafunction User Guide*.

Document Revision History

Table 8-9 lists the revision history for this chapter.

Table 8-9. Document Revision History (Part 1 of 2)

Date	Version	Changes Made
December 2011	4.2	<ul style="list-style-type: none"> ■ Updated “Differential Receiver” section. ■ Minor text edits.
June 2011	4.1	<ul style="list-style-type: none"> ■ Updated Figure 8-2. ■ Minor text edits.
December 2010	4.0	Updated for the Quartus II software version 10.1 release: <ul style="list-style-type: none"> ■ Added Arria II GZ device information. ■ Updated Table 8-3 and Table 8-4. ■ Updated Figure 8-2.

Table 8–9. Document Revision History (Part 2 of 2)

Date	Version	Changes Made
July 2010	3.0	Updated for Arria II GX v10.0 release: <ul style="list-style-type: none"> ■ Updated Table 8–1 and Table 8–2. ■ Updated Figure 8–1 and Figure 8–5. ■ Updated “Non-DPA Mode” section. ■ Removed Table 8–1: Supported Data Range. ■ Minor text edit.
November 2009	2.0	Updated for Arria II GX v9.1 release: <ul style="list-style-type: none"> ■ Updated Table 8–1 and Table 8–2. ■ Updated Figure 8–1. ■ Updated “LVDS Channels” and “Non-DPA Mode” sections. ■ Minor text edit.
June 2009	1.1	<ul style="list-style-type: none"> ■ Updated Table 8–2 and Table 8–3. ■ Updated “Programmable Pre-Emphasis and Programmable VOD.” and “LVDS Channels” sections.
February 2009	1.0	Initial release

