

## Core Overview

The Avalon® Streaming (Avalon-ST) Serial Peripheral Interface (SPI) core is an SPI slave that allows data transfers between SOPC Builder systems and off-chip SPI devices via Avalon-ST interfaces. Data is serially transferred on the SPI, and sent to and received from the Avalon-ST interface in bytes.

The SPI Slave to Avalon Master Bridge is an example of how this core is used. For more information on the bridge, refer to the *SPI Slave/JTAG to Avalon Master Bridge Cores* chapter in volume 5 of the *Quartus II Handbook*.

The Avalon-ST Serial Peripheral Interface core is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system.

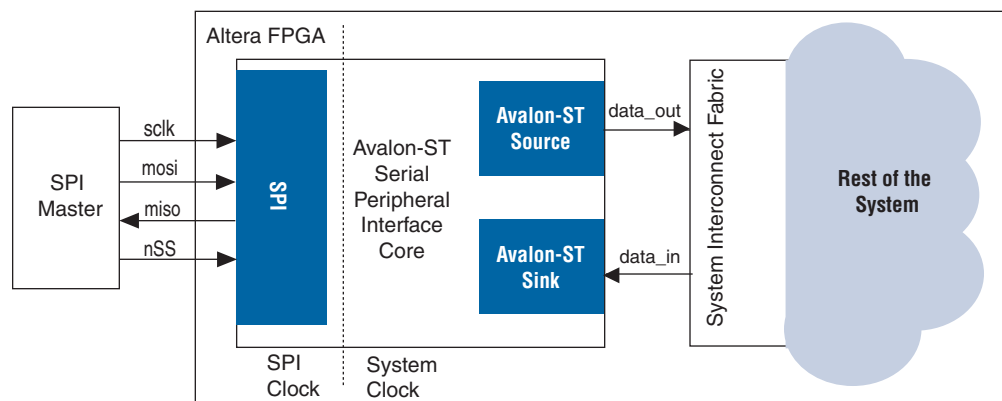
This chapter contains the following sections:

- “Functional Description”
- “Instantiating the Core in SOPC Builder” on page 10–3
- “Device Support” on page 10–3

## Functional Description

Figure 10–1 shows a block diagram of the Avalon-ST Serial Peripheral Interface core in a typical system configuration.

**Figure 10–1.** SOPC Builder System with an Avalon-ST SPI Core



## Interfaces

The serial peripheral interface is full-duplex and does not support backpressure. It supports SPI clock phase bit, CPHA = 1, and SPI clock polarity bit, CPOL = 0.

Table 10-1 shows the properties of the Avalon-ST interfaces.

**Table 10-1.** Properties of Avalon-ST Interfaces

Feature	Property
Backpressure	Not supported.
Data Width	Data width = 8 bits; Bits per symbol = 8.
Channel	Not supported.
Error	Not used.
Packet	Not supported.



For more information about Avalon-ST interfaces, refer to the [Avalon Interface Specifications](#).

## Operation

The Avalon-ST SPI core waits for the `nss` signal to be asserted low, signifying that the SPI master is initiating a transaction. The core then starts shifting in bits from the input signal `mosi`. The core packs the bits received on the SPI to bytes and checks for the following special characters:

- `0x4a`—Idle character. The core drops the idle character.
- `0x4d`—Escape character. The core drops the escape character, and XORs the following byte with `0x20`.

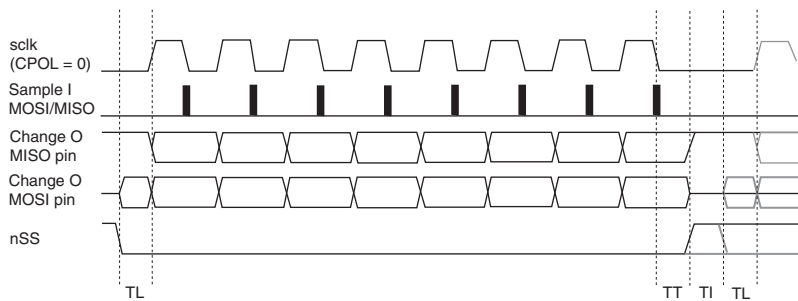
For each valid byte of data received, the core asserts the `valid` signal on its Avalon-ST source interface and presents the byte on the interface for a clock cycle.

At the same time, the core shifts data out from the Avalon-ST sink to the output signal `miso` beginning with from the most significant bit. If there is no data to shift out, the core shifts out idle characters (`0x4a`). If the data is a special character, the core inserts an escape character (`0x4d`) and XORs the data with `0x20`.

The data shifts into and out of the core in the direction of MSB first.

Figure 10-2 shows the SPI transfer protocol.

Figure 10-2. SPI Transfer Protocol



Notes to Figure 10-2:

- (1) TL = The worst recovery time of `sclk` with respect with `nSS`.
- (2) TT = The worst hold time for `MOSI` and `MISO` data.
- (3) TI = The minimum width of a reset pulse required by Altera FPGA families.

## Timing

The core requires a lead time (TL) between asserting the `nSS` signal and the SPI clock, and a lag time (TT) between the last edge of the SPI clock and deasserting the `nSS` signal. The `nSS` signal must be deasserted for a minimum idling time (TI) of one SPI clock between byte transfers. A TimeQuest SDC file (`.sdc`) is provided to remove false timing paths. The frequency of the SPI master's clock must be equal to or lower than the frequency of the core's clock.

## Limitations

Daisy-chain configuration, where the output line `miso` of an instance of the core is connected to the input line `mosi` of another instance, is not supported.

## Instantiating the Core in SOPC Builder

Use the MegaWizard™ interface for the Avalon-ST SPI core in SOPC Builder to add the core to a system. The parameter **Number of synchronizer stages: Depth** allows you to specify the length of synchronization register chains. These register chains are used when a metastable event is likely to occur and the length specified determines the meantime before failure. The register chain length, however, affects the latency of the core.



For more information on metastability in Altera devices, refer to [AN 42: Metastability in Altera Devices](#). For more information on metastability analysis and synchronization register chains, refer to the [Area and Timing Optimization](#) chapter in volume 2 of the *Quartus II Handbook*.

## Device Support

The Avalon-ST SPI core supports all Altera® device families.

## Referenced Documents

This chapter references the following documents:

- *Avalon Interface Specifications*
- *SPI Slave/JTAG to Avalon Master Bridge Cores* chapter in volume 5 of the *Quartus II Handbook*
- *AN 42: Metastability in Altera Devices*
- *Area and Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*

## Document Revision History

Table 10-2 shows the revision history for this chapter.

**Table 10-2.** Document Revision History

Date and Document Version	Changes Made	Summary of Changes
November 2009 v9.1.0	Added a description to specify the shift direction.	—
March 2009 v9.0.0	Added description of a new parameter, <b>Number of synchronizer stages: Depth.</b>	—
November 2008 v8.1.0	Changed to 8-1/2 x 11 page size. No change to content.	—
May 2008 v8.0.0	Initial release.	—